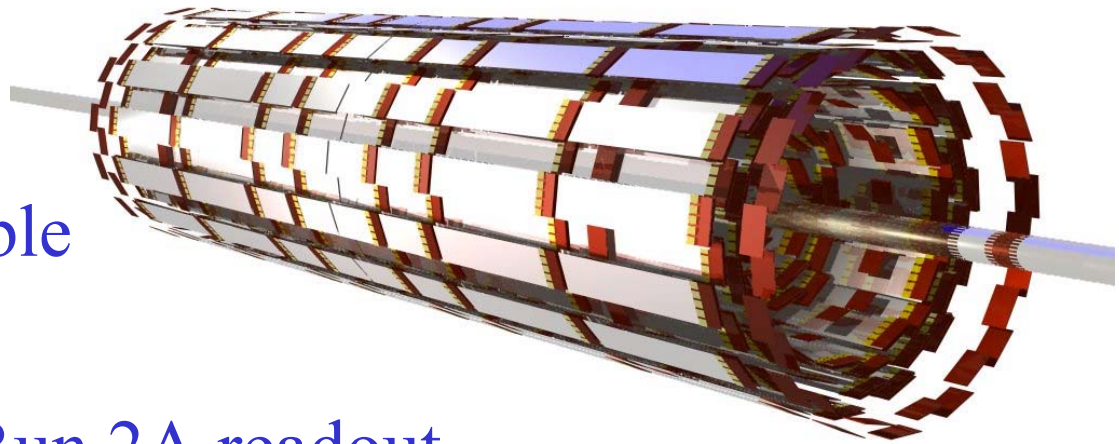
Run 2B Silicon Electronics & Readout

Andrei Nomerotski, Fermilab

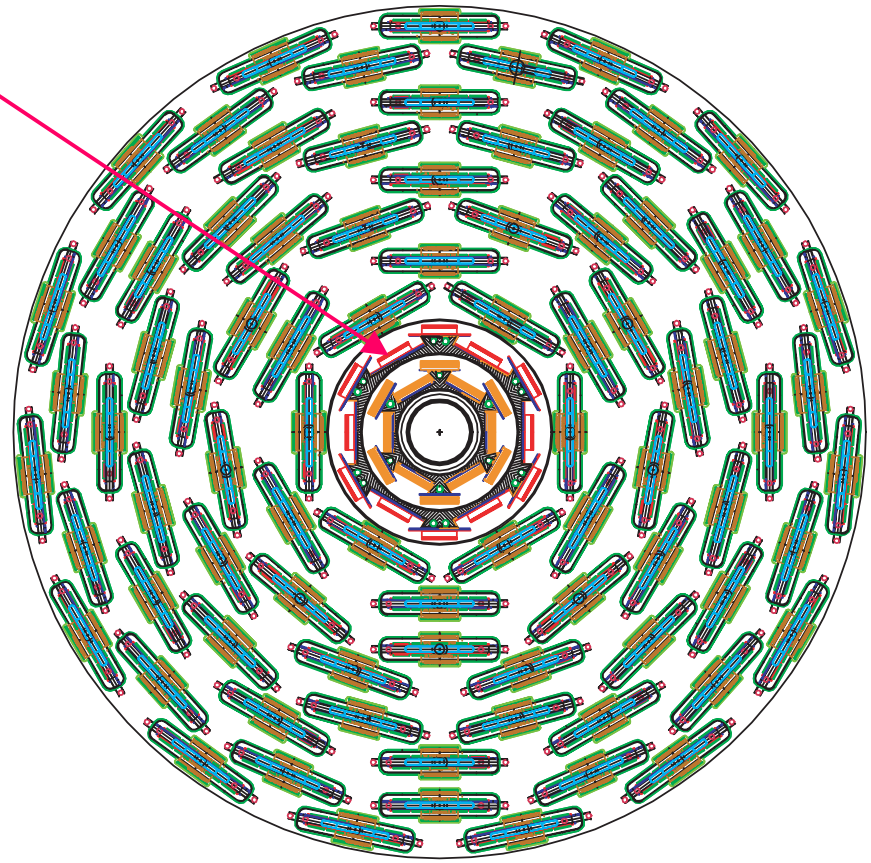
April 26 2002, Collaboration meeting

- Overview
- SVX4 chip
- Analog flex cable
- Hybrids
- Interfacing to Run 2A readout
- Plans for 2002
- Summary

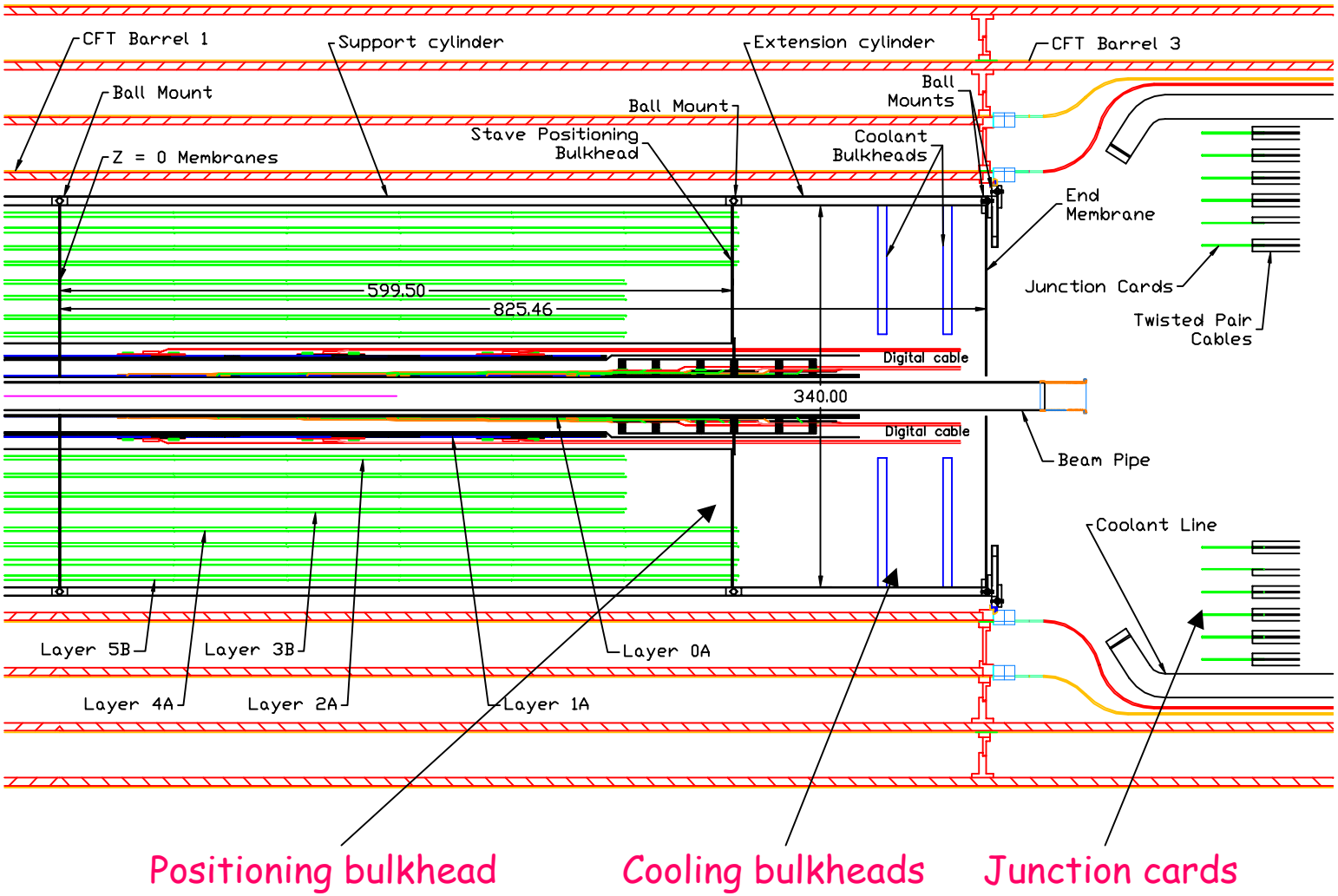


Run 2B Silicon Layout

- Six layer silicon tracker, divided in two radial groups
  - Inner layers: Layers 0 and 1
    - ❖ Axial readout only
    - ❖ Mounted on integrated support
    - ❖ Assembled into one unit
    - ❖ Designed for V_{bias} up to 700 V
  - Outer layers: Layers 2-5
    - ❖ Axial and stereo readout
    - ❖ Stave support structure
    - ❖ Designed for V_{bias} up to 300 V
- Employ single sided silicon only, 3 sensor types
  - 2-chip wide for Layer 0
  - 3-chip wide for Layer 1
  - 5-chip wide for Layers 2-5



Silicon Detector Layout

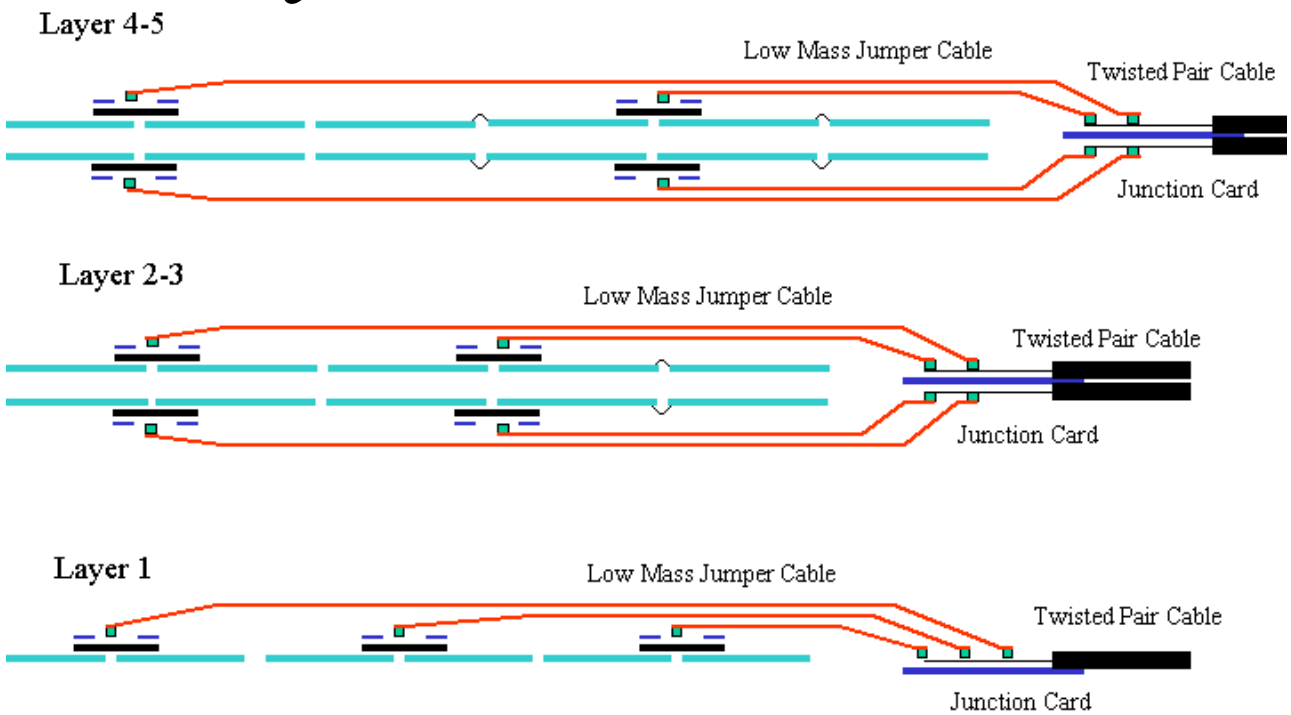


Readout

- Run2B Silicon readout is based on
  - new SVX4 chip
  - Run 2A readout with minimal modifications
  - Conservative, low risk solutions with minimum R&D
- Baseline established in September 2001
  - Went through several reviews
  - Steady progress last months
  - Conceptual design stage evolved to detailed design & prototyping stage
- In the following will concentrate on latest developments
  - Up to date documentation

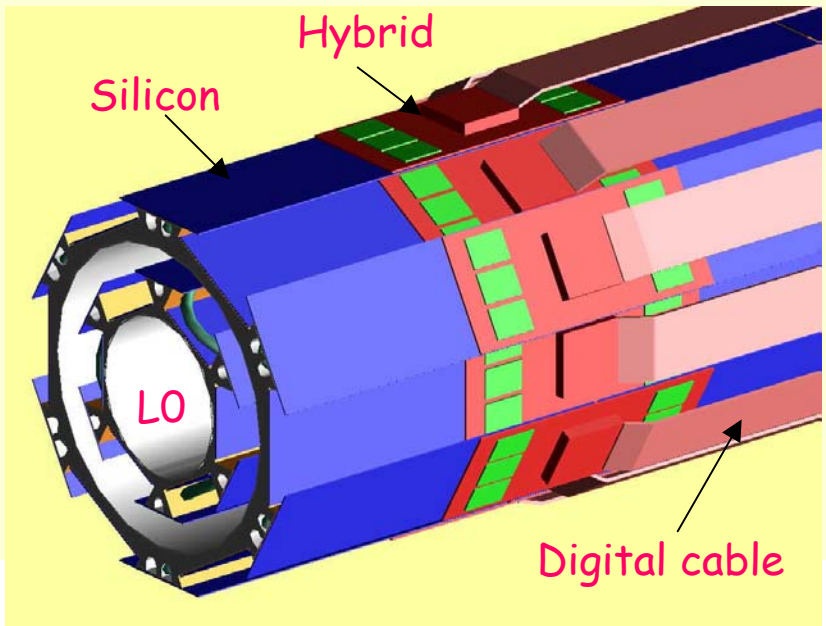
    http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/readout/readout.html

Layers 1 - 5 Readout

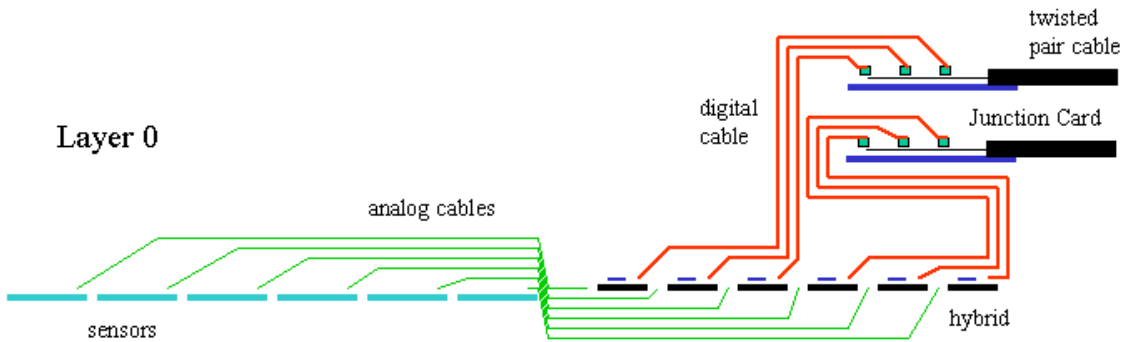


- On-board double-ended beryllia hybrid
- Reduction of readout cables is achieved by
  - Analog ganging : connected strips in L2-5
  - Digital ganging : chips bonded to different sensors are daisy chained on hybrid in L1-5
- Low mass digital flex (jumper) cable with connectors on both sides

Layer 1

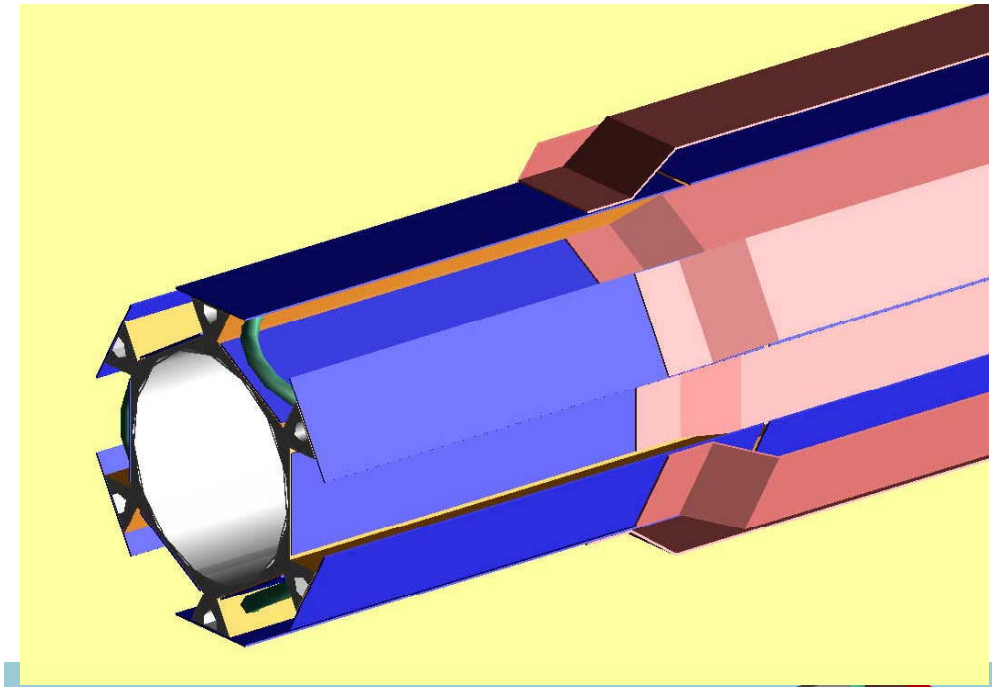


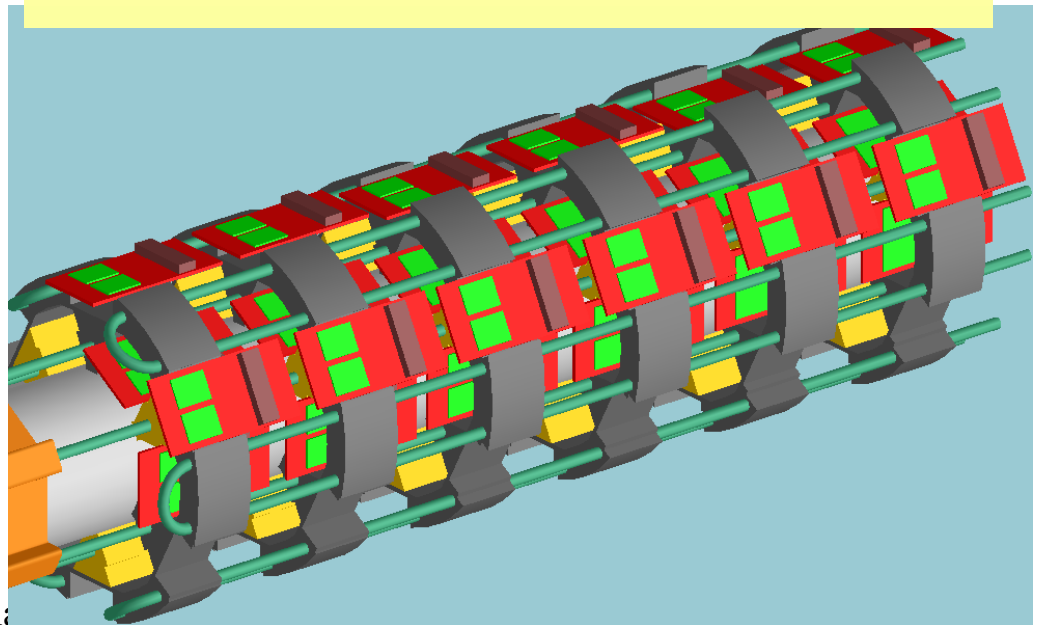
Layer 0 Readout



- small radius & minimal material => flex analog cables
- flex length is equalized
- two-chip hybrids, no ganging
- beyond hybrid : identical to L1
- challenging :
  - noise performance
  - manufacturing and assembly

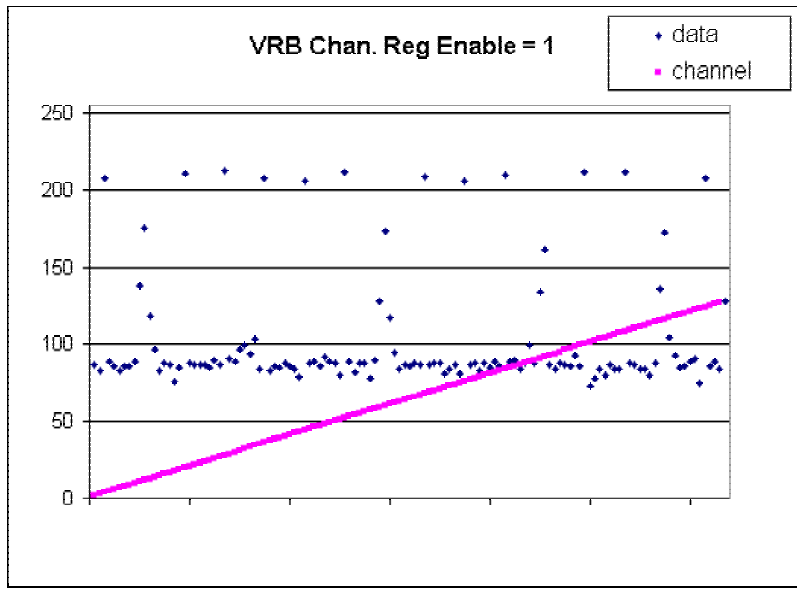
Layer 0





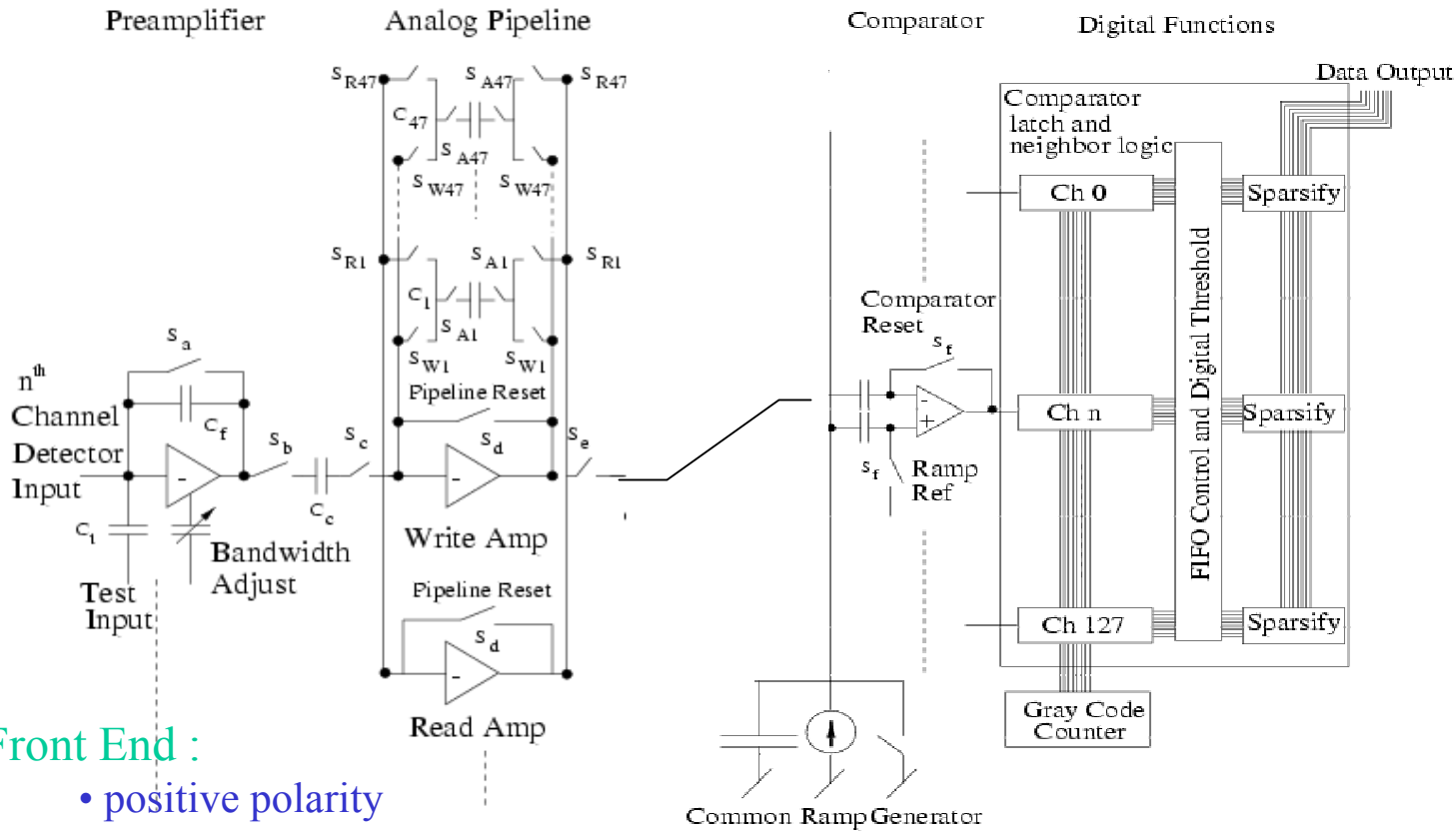
SVX4 Chip

- New chip : SVX4
  - Designed by Fermilab/LBL/Padua
  - 0.25 μm technology, intrinsically radiation hard
  - Based on SVX3, compatible with SVX2
  - Several new schematics solutions
  - D0 will use differential readout
    - ❖ Use the same pad ring as CDF
- D0 DAQ can operate with SVX3 chips
  - D0 DAQ was designed for SVX2
  - Some remapping of control signals is required
  - Tested in Nov 2000, one SVX3 chip was read out with D0 Sequencer



SVX3 Address & Data, 128 channels

SVX4 Chip



Front End :

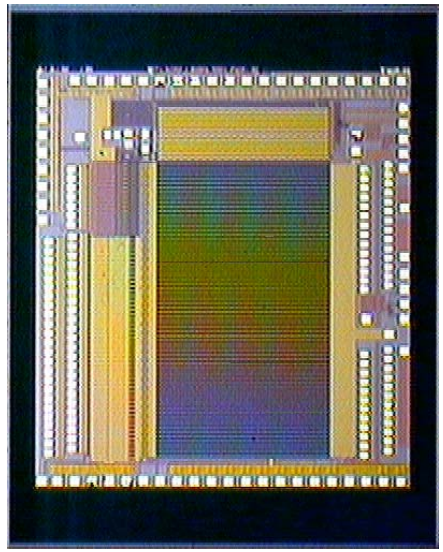
- positive polarity
- gain 3 mV/fC, 5% uniformity
- load 10 – 40 pF
- risetime 60-100 nsec
- dynamic range 200 fC
- ‘black hole’ clumping
- reset time 200 nsec
- pipeline 42 cells

Back End :

- Wilkinson ADC, 106 MHz counter
- dynamic pedestal subtraction
- data sparsification
- neighbor logic
- differential output drivers upto 17 mA
- configuration register

SVX4 Chip

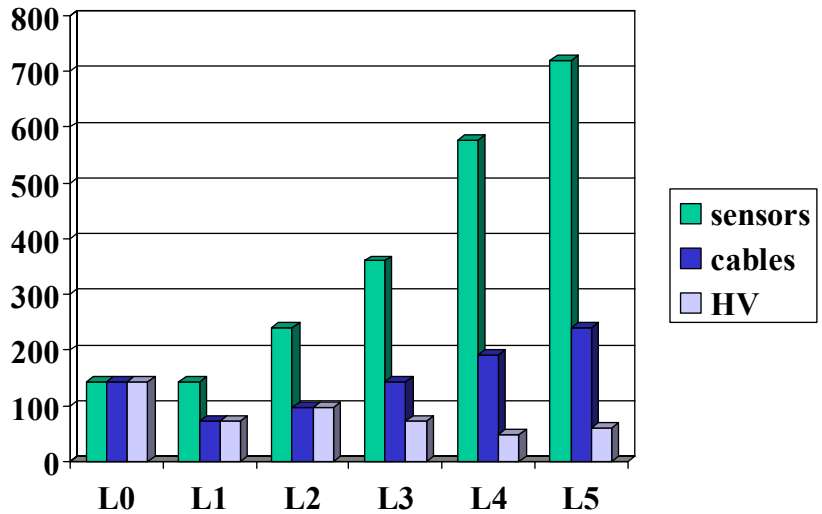
- Front End design completed in June 2001
  - FE test chip tested in September 2001
  - Optimum preamp ENC = 450e + 43.0e/pF
  - Pipeline validated
  - Excellent radiation hardness
- Full chip layout and simulation completed in March 2002
  - Prototype submitted to MOSIS on March 28 2002
  - Two versions for prototyping
    - ❖ Conservative
    - ❖ On-chip bypassing of analog voltage
  - Chip dimensions 9.17 mm x 6.42 mm, power < 0.5W/chip
  - Chips back from TSMC on May 23rd, available for tests in June 2002, will have ~240 chips of each version
- Joint test effort of CDF & D0 at LBL and Fermilab
  - Important to test prototypes as extensively as possible to minimize extra submissions
- Production run planned in April 2003
  - Second prototype submission is assumed in the schedule



FE test chip

Cable Count

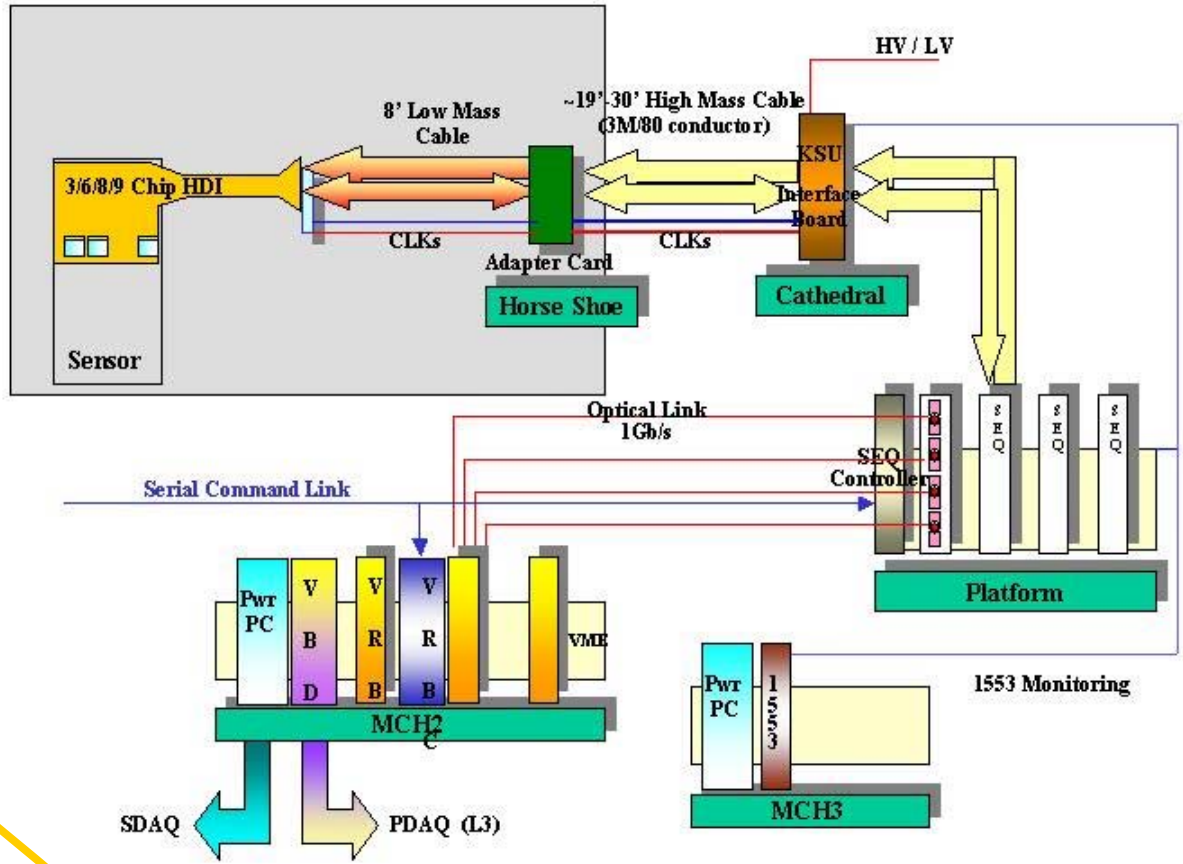
Layer	SVX4/Hybrid	# readout cables	# HV cables
0	2	144	144
1	6	72	72
2	10	96	96
3	10	144	72
4	10	192	48
5	10	240	60
all layers		**888**	**492**
Run 2A		**912**	**440 +**



# of sensors and cables per layer

Run 2B readout cable count is smaller than Run 2A cable count

Changes of Run 2A Readout

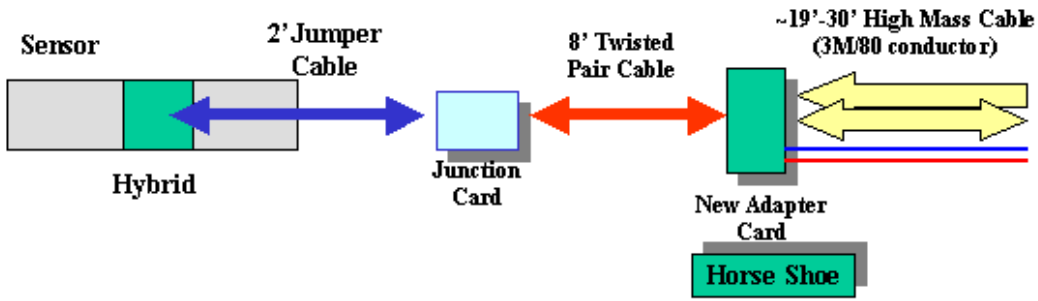


Modifications

- Signal level translation 5 V – 2.5 V
- Tight spec on 2.5 V (2.25 – 2.75 V) => Voltage regulation
- Mapping between SVX4 and SVX2
- Differential / Single-Ended translation
- Some changes in LV / HV power supplies, Interface Crates

Run 2B Readout

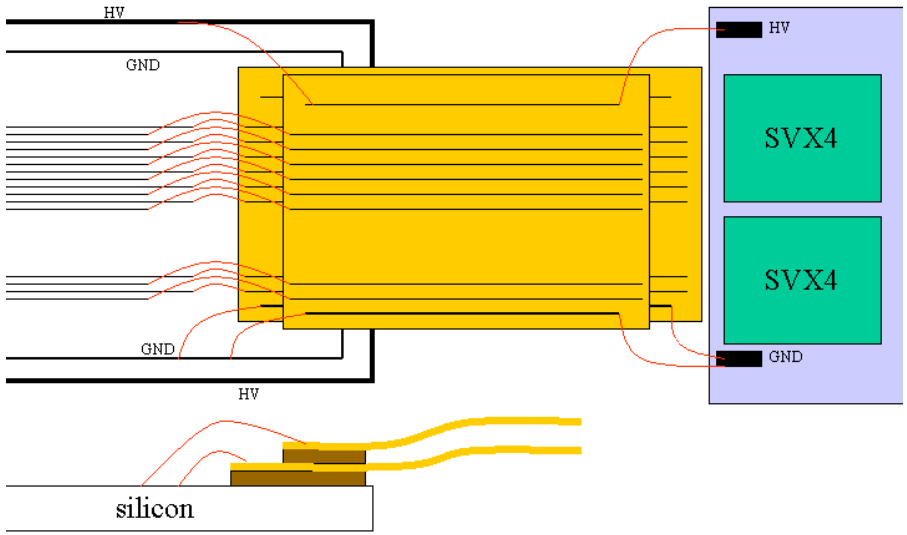
- Preserve Run 2A segmentation of readout :
  - One hybrid is an independent unit (separate cable) up to an accessible region.
    - ❖ Proven to be successful during Run 2A commissioning.



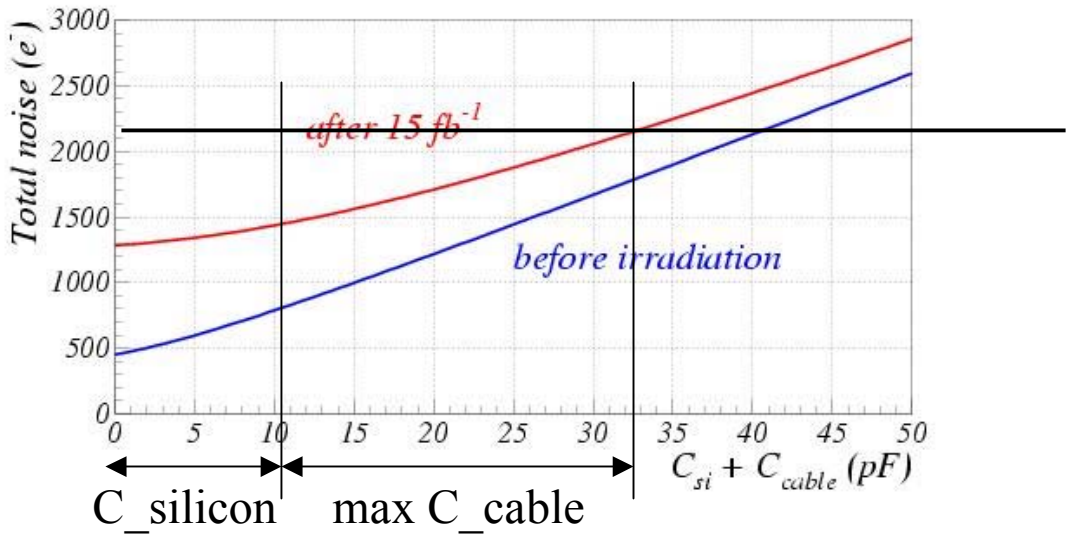
- Jumper Cable - Junction Card - Twisted Pair Cable – **Adapter Card**
- New Adapter Card is active, implements necessary modifications
- Junction Cards are located in an accessible area
- Twisted Pair Cable is well suited for differential SVX4 readout

Analog Flex Cables

- Low mass, fine pitch cables for Layer 0
  - Trace width 15-20 um
  - Constant 100 um pitch without fan-out region
  - Two cables shifted by 50 um, effective pitch 50 um matches sensor pitch



L0 noise performance



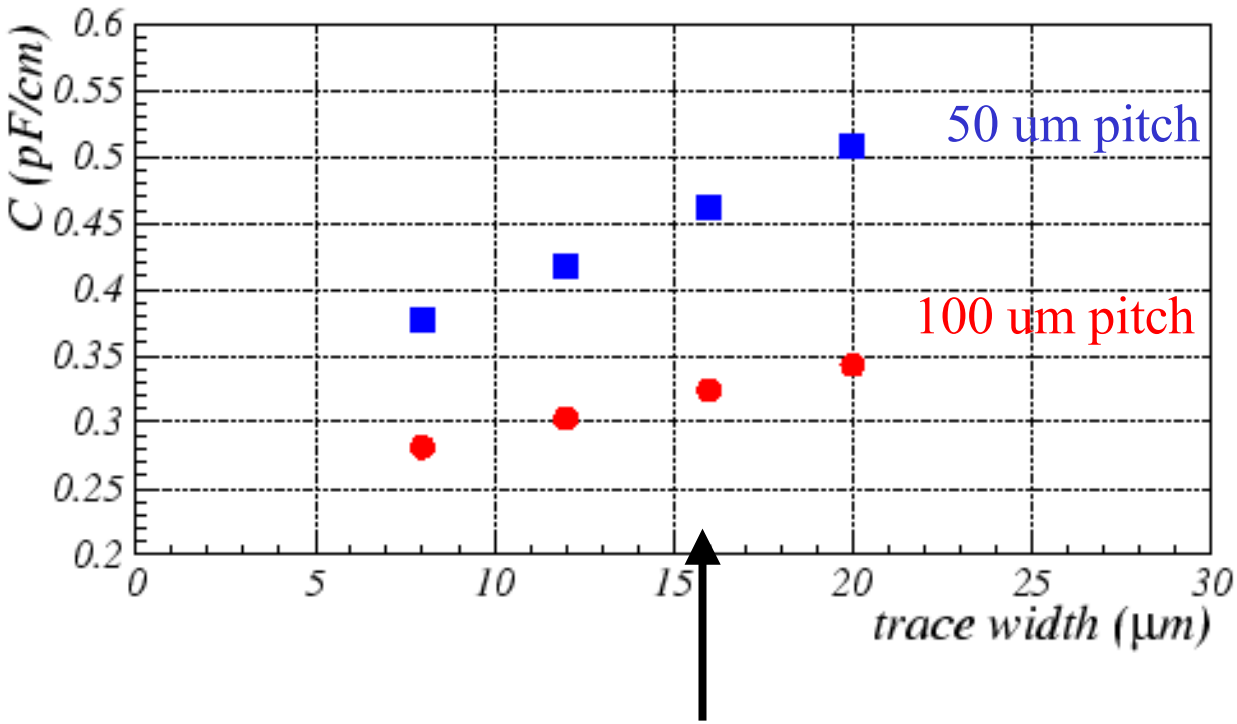
S/N =10

Acceptable cable capacitance is determined by noise performance

S/N = 10 after 15 fb-1 => C_cable < 0.55 pF/cm for 42 cm long cable
typical C_silicon ~ 1.2 pF/cm

L0 Analog Cable Capacitance

- FE calculations (ANSYS) agree with measurements within 10%
- 50 μm thick substrate with $\varepsilon_r = 3.5$
- Settled on 91 um pitch and 16 um trace width



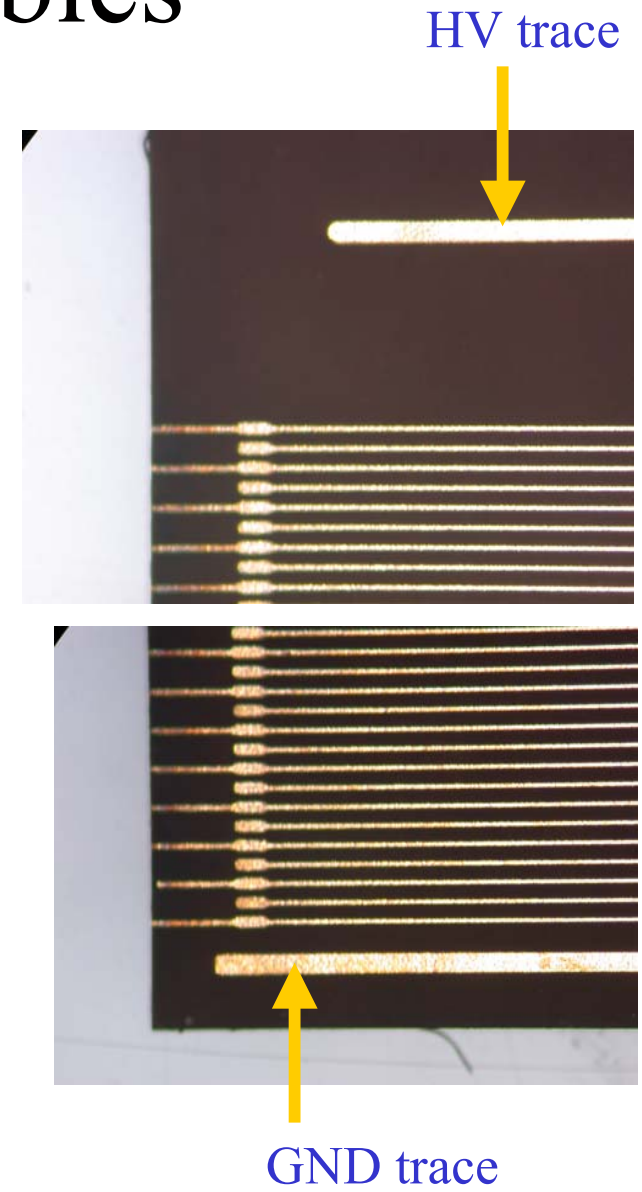
16 um => 0.32 pF/cm

Analog Flex Cables

- Dyconex
  - Designed by Fermilab, Universitaet Zuerich
  - Second prototype run (March 2002)
    - ❖ pitch 91 um, trace width 16 um
    - ❖ Used regular etching technology
    - ❖ 15 mechanical grade cables
    - ❖ 12 good cables
    - ❖ More cables ready in April
  - Results on the 12 good cables:
    - ❖ Good quality of imaging
    - ❖ Allow one open tra[illegible]129

Open traces	0	1	2	>2
cables	6	4	2	0

    - ❖ Measured trace width : 9-14 μm
    - ❖ Capacitance, resistance measurements under way
      - ❖ Preliminary C=0.39 pF/cm
- Compunetics
  - Run2A SMT HDI & CFT VLPC cable vendor
  - Placed order for 20 cables, same design
    - ❖ Ready in May

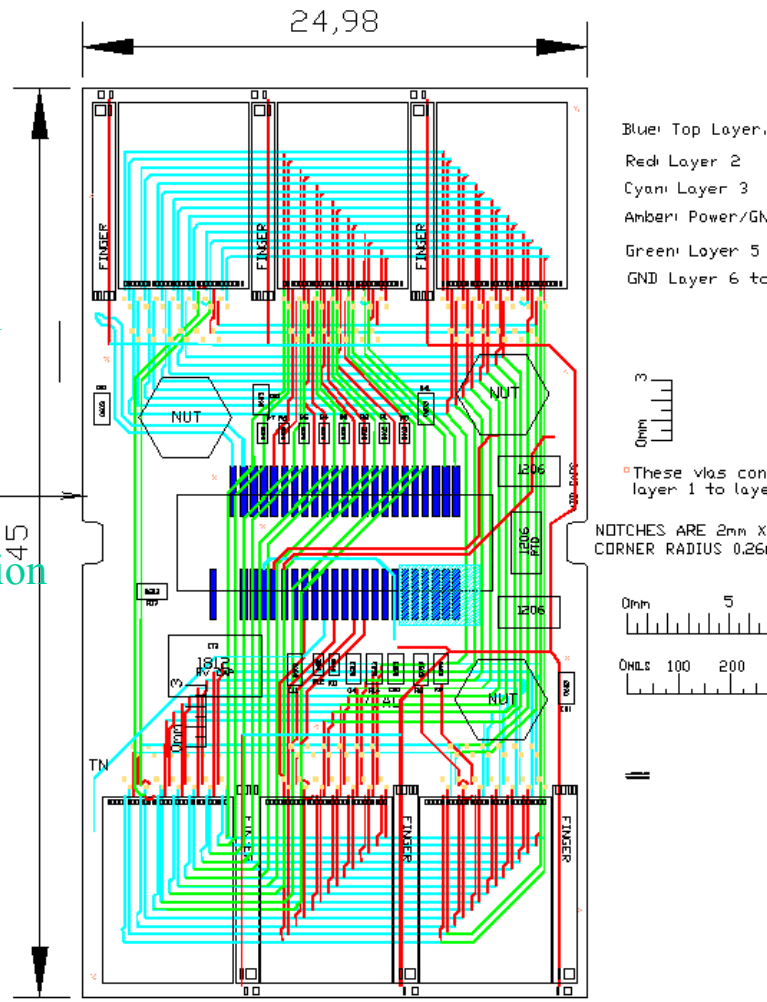


Hybrids

- Based on Beryllia ceramic
  - Minimize material, BeO thickness 0.38 mm
  - Good heat conductor
  - Established technique
- Multilayer structure on the substrate
  - six Au layers
    - ❖ GND & power planes, 4 um thick
    - ❖ Traces, 8 um thick, 100 um wide
  - five 40 um dielectric layers, total thickness 0.8 mm
  - Two technologies for vias in dielectric
    - ❖ Etching (Fodel dielectric), min via size 4 mils
    - ❖ Screen printing, min via size 8 mils
  - Screen printing is our baseline
    - ❖ Cost effective
    - ❖ More vendors capable to screen print on BeO
      - CPT, Oceanside CA - used by CDF
      - ALDEN, Alden NY
      - AMITRON, North Andover MA
      - Hybrid Microcircuits, Blue Earth MN – used by CLEO

Hybrids

- Four types of hybrids
  - Layer 0 : 2 chips
  - Layer 1 : 6 chips, double-ended
  - Layers 2-5 : 10 chips, double-ended
    - Axial
    - Stereo, different width, electrically identical to axial
- For all hybrids
  - ~10 mil spacing between vias
  - 50 pin AVX 5046 connector, 3 mm high
    - Allows for easy testing during all phases of production and assembly
    - Used by CDF for Run 2A SVX
  - Fingerless design
  - bypass capacitors, termination resistors
  - temperature sensor
  - HV routed to side pin with 4 neighbors removed, tested to 1600 V
  - Reserved space (“nuts”) for assembling purposes

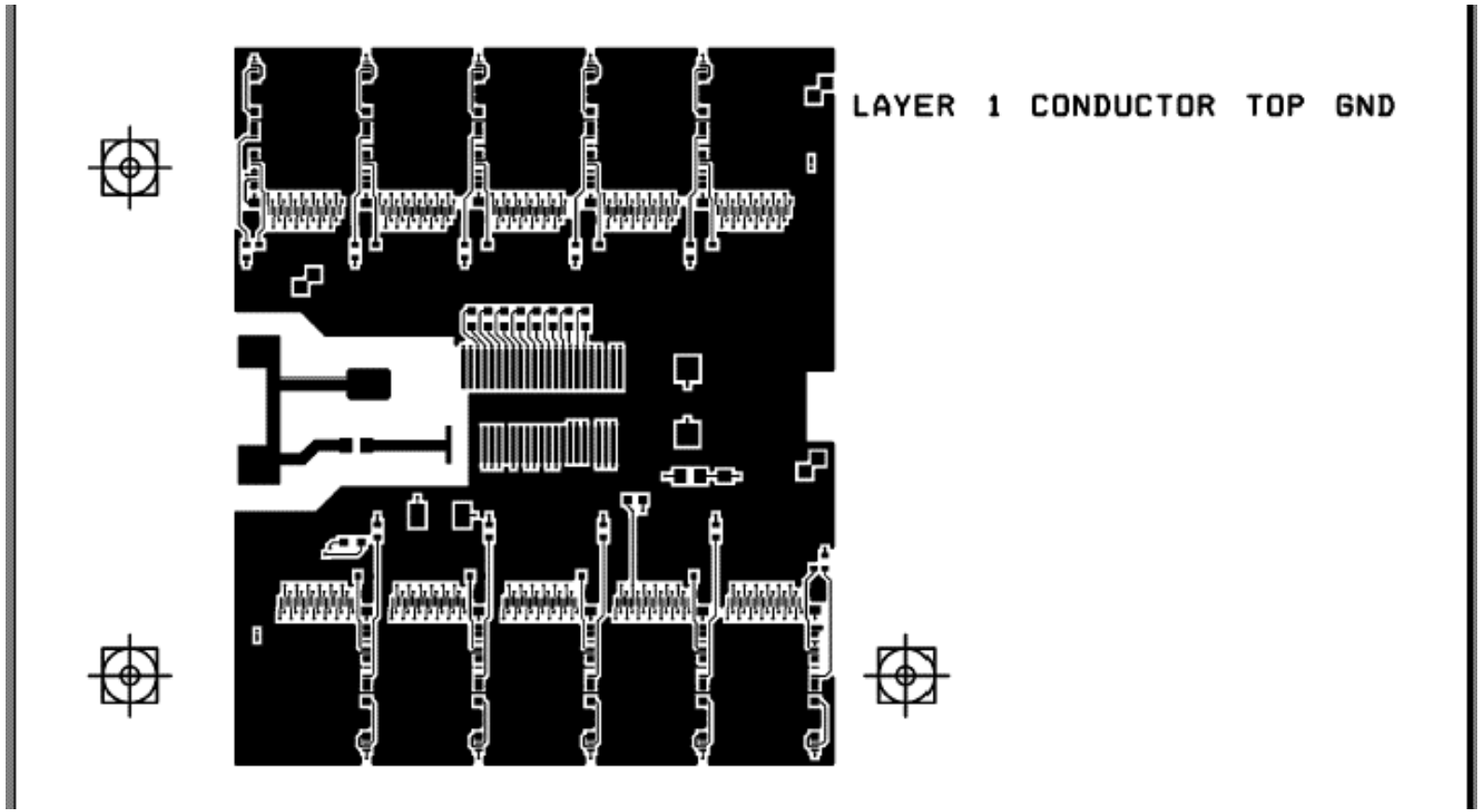


Layer 1 hybrid layout

Hybrids

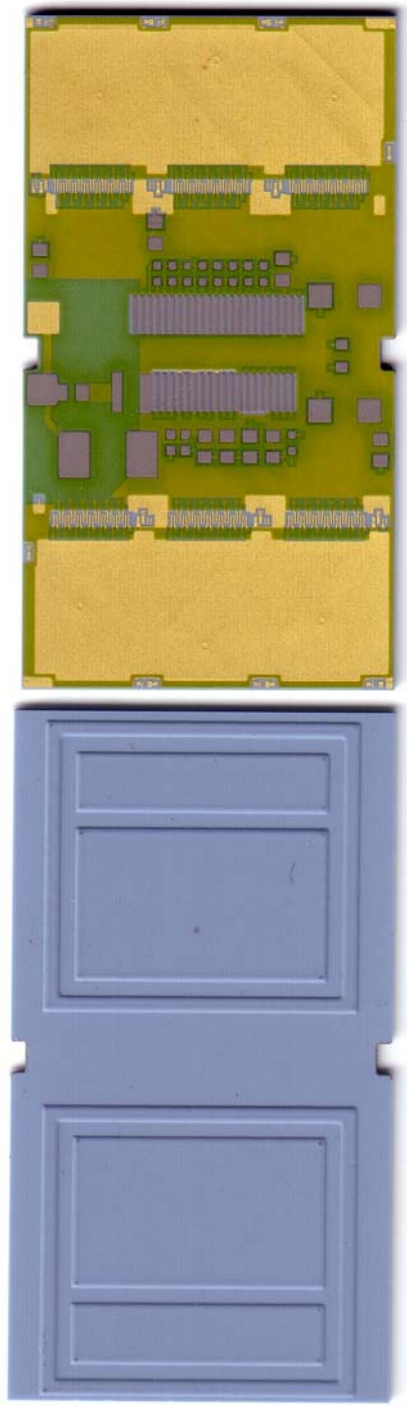
Layers 2-5 10-chip hybrid :

Design similar to Layer 1 6-chip hybrid



Hybrids

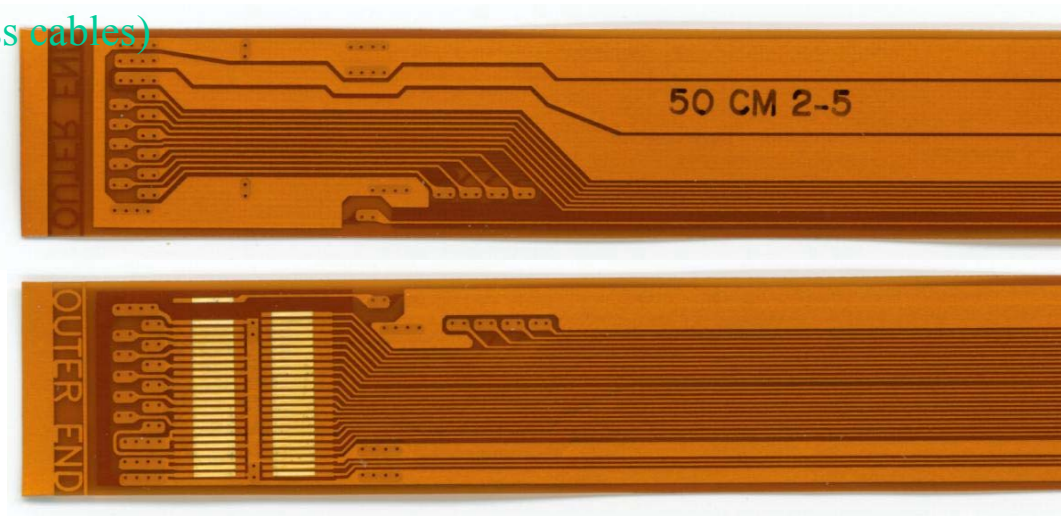
- Designed by Fermilab
- Ordered prototypes for Layer 1 from CPT in January 2002
  - 18 hybrids are ready, received 8 last week
- Going ahead with tests @ U.Kansas, CSU Fresno, Fermilab
  - Mechanical (thickness, flatness, dimensions, gluing)
    - ❖ Flatness 40 um (spec 50 um)
  - Stuffing and bonding
  - Electrical
    - ❖ Probing to validate the layout and quality
    - ❖ Other tests when SVX4 are available
- Ordering L2A and L2S hybrids
  - Layouts are ready
  - Two hybrids (one L2A & L2S) per BeO substrate
  - Two vendors : CPT and Amitron
  - Prototypes ready in July



Digital Jumper Cable

Hybrid - **Jumper Cable** - Junction Card - Twisted Pair Cable – Adapter Card

- Designed by Kansas State
- Same design for all layers
  - 10-12 different lengths, max length ~ 1 m
  - Kapton substrate, total thickness 250 um for L0-1, 330 um for L2-5
  - HV on the same cable
  - AVX 50-pin connector on both sides
- Layout reviewed and prototypes ordered in January 2002
  - From Honeywell (Run2A low mass cables)
  - Back in March 2002, look good
  - Electrical, mechanical tests proceeding
- Second vendor :Basic Electronics
  - Placing order

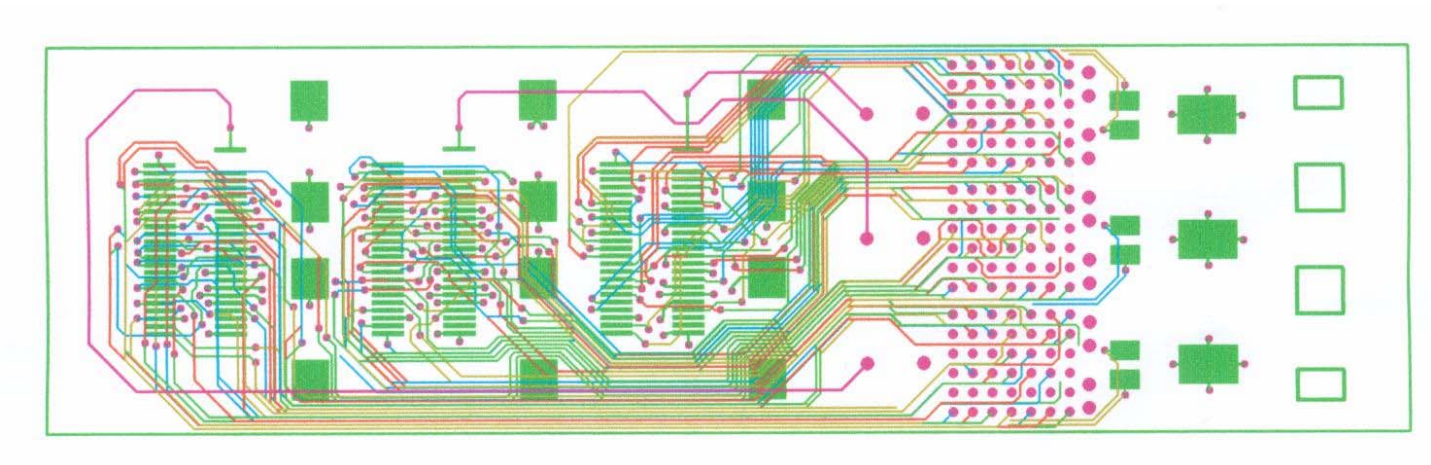


Junction Card

Hybrid - Jumper Cable - **Junction Card** - Twisted Pair Cable – Adapter Card

- L0-1 : 3 hybrids → junction card
  L2-5 : 2 hybrids → junction card
- 50-pin AVX connectors,
  three(two) receptacles heights: 3.0, 3.5, (3.0) mm
- Twisted pairs are soldered to JC,
  cards are extensions of cable bundles
- Dimensions 97 (70) mm x 25 mm

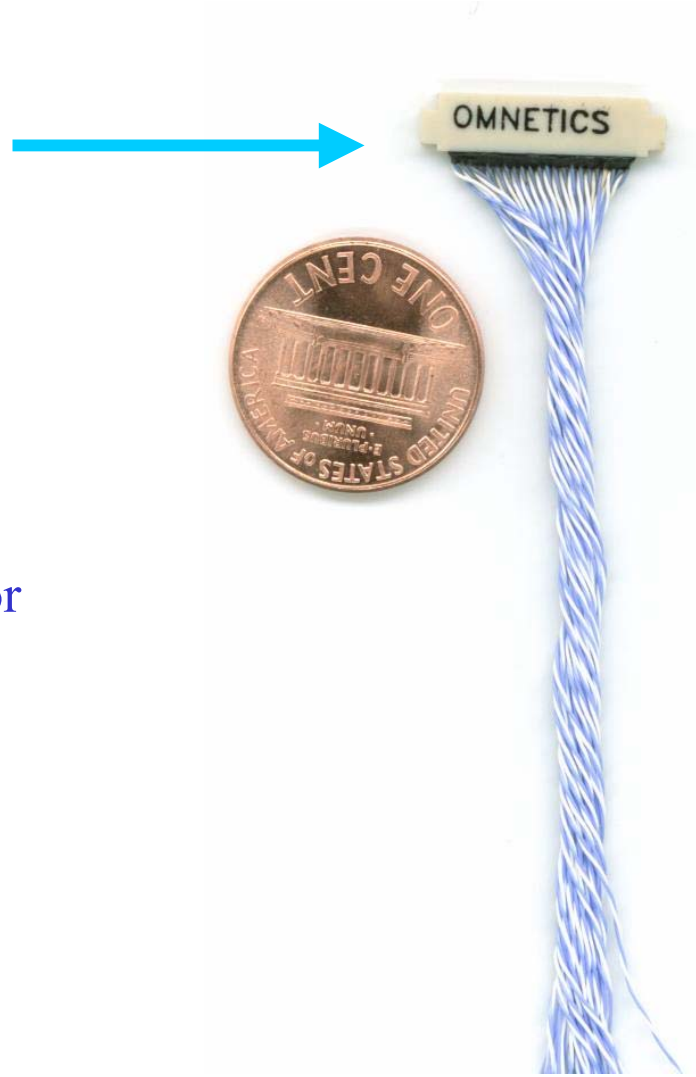
- Designed by Kansas State
- Layout reviewed in March 2002
- Prototypes ordered in April 2002
- Ready for testing in May 2002



Twisted Pair Cable

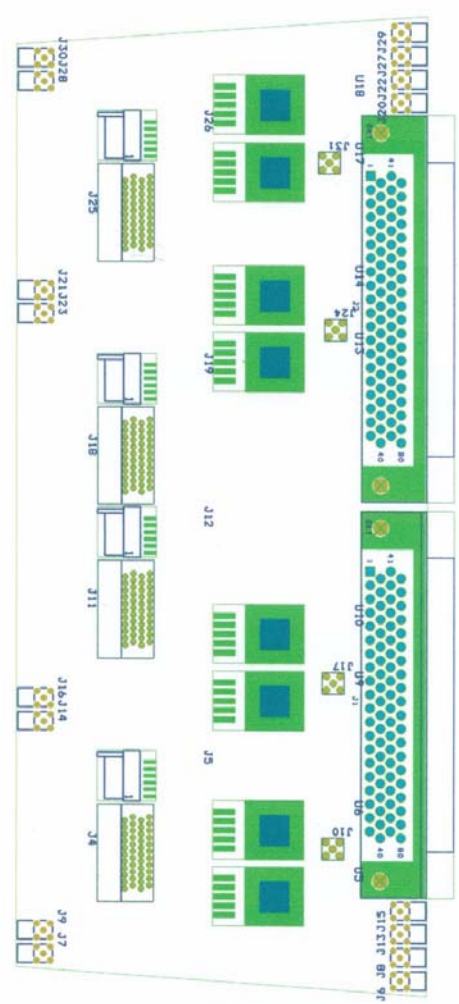
Hybrid - Jumper Cable - Junction Card - **Twisted Pair Cable** – Adapter Card

- Consists of
  - Signal pairs : 44-pin Omnetics connector
  - Power & HV lines : 6-pin Omnetics connector
  - Clock coaxes
- Designed by Fermilab
- Design reviewed in February
- All parts (connectors, pairs) ordered for prototype cables
- Prototypes ready in July



Adapter Card

Hybrid - Jumper Cable - Junction Card - Twisted Pair Cable – **Adapter Card**



Top view of 4-channel Adapter Card

- Adapter Card is active :
  - Two voltage regulators per hybrid: analog and digital voltages
  - Differential-to-Single-Ended 2.5-to-5 V translation for SVX4 Data
  - 5-to-2.5 V translation for SVX4 Controls
  - Routing of Clock and HV
- Three rings of Adapter Cards at two ends of calorimeter
- Designed by Kansas State
- Design reviewed on April 22, some changes needed
- Prototypes ready in July

Interface Board & Power Supplies

- Baseline : retain Run 2A IB's, use in full functionality
  - Signal regeneration and termination
  - LV distribution
  - LV voltage/current monitoring
  - HV distribution for L2-5 (< 300 V)
  - Hybrid Enable/Disable
  - Hybrid temperature monitoring
  - Current & temperature protection
- Will need small modifications of IB inputs (terminations)
- Note: Present IB fixes several SVX2 "features"
  - Assumption : SVX4 will not have new "features" which cannot be recovered with present IB
- LV power supplies and Grounding issues were topics of April 22nd workshop

High Voltage

- Current caused by radiation damage
  - Assume 15 fb-1, -10 deg C

Layer	Radius,mm	uA/strip	uA/hybrid	uA/stave	Hybrids/HV ch
0	18	1.2	310	NA	1
1	35	0.46	360	NA	1
2	54	0.28	530 max	1790	1
3	86	0.12	230 max	770	2
4	116	0.06	180 max	550	4

  - Max current < 0.6 mA
  - Total HV channel count of 492
  - Will keep the present HV system : Bira 2000 V, 3.2 mA
  - Currently have 10 crates, 440 HV channels (out of them 248 are positive)
  - Will have 11 crates; 528 positive channels
    - Mexican collaborators (CINVESTAV) are buying the balance between Run2A and Run2B in 2002
  - Will need partly new cable plant and distribution system

Status

Component	Vendor	Design	First Prototype		Second Prototype		Final
			Ordered	Delivered	Ordered	Delivered	Order
SVX4	TSCM	✓	✓				
Analogue Cable	Dycx	✓	✓	✓	✓	✓	
	Comp	✓	✓				
L0 Hybrid		50%					
L1 Hybrid		✓	✓				
L2A Hybrid		✓					
L2S Hybrid		✓					
Digital Cable	Honey	✓	✓	✓			
	Basic	✓					
Junction Card		✓	✓	✓			
Twisted Pr. Cable		✓	✓				
Adapter Card		75%					
Test Stand Elctr.		✓					
High Voltage		✓					✓

Performance issues

- Readout time is important issue in deadtime accounting
- Simulations :
  - Two-jet events
  - Run 2B GEANT
  - Realistic clustering
  - Neighbors and noise contribution

Layer	S/N	Max # strips	Readout Time, usec
0	8	95	3.8
1	15	85	3.4
2	15	70	2.8

- Maximum # of strips read out per cable
  - Allows for comparison between layers
- Readout time is comparable for first three layers
  - Assumes low S/N in Layer 0 after radiation damage
  - Justifies 2-chip readout for Layer 0
- Deadtime is still dominated by digitization and pipeline reset (~7.2 usec).
  - Unavoidable in D0 DAQ architecture
  - Total deadtime, ~11-12 usec, is acceptable.

Electronics & Readout in 2002

- Major milestones in 2002
  1. SVX4 tests
     - Bare chip tests : starting June 2002
     - Hybrid tests : starting July 2002
  2. Full chain tests : starting September 2002
  3. L0 prototype with Analog cable : fall 2002
- Goal :

  sign-off on all components for production in 2002

Summary

- Have a baseline for Run 2B Silicon Readout
- Good group of people (KSU, KU, Fresno, Zurich, Fermilab)
- Excellent progress last months
- Detailed design exist for (almost) all components
- Moved on to prototyping
  - Have some prototypes in hand (L1 hybrid, Digital flex cable)
  - All prototype components for full readout chain test ready by September 2002
- Exciting time still ahead

  SVX4 tests starts June 1!